C2 in accordance with a Gray code sequence for reducing jitter when the phase control word change states.

22. (Unchanged) The timing circuit according to claim 21, wherein the phase control word has a characteristic width J, where J is mathematically dependent on the frequency scale factor M.

REMARKS

The present invention is a unique high-speed, low-jitter, high-phase resolution Phase Lock Loop (PLL) circuit. In the present device, a timing reference signal generator, such as a voltage controlled oscillator (VCO), is connected in feedback fashion in order to provide a timing reference signal to the detector. The timing reference signal generator is operatively configured to oscillate and thereby produce an output signal at a characteristic frequency which is an integral multiple (M) of a desired output clock frequency. Moreover, a loop filter coupled between the phase/frequency detector and the timing reference signal generator is used to develop a control voltage for controlling the operational frequency of the VCO. The number of phases represented by the multi-phase output signals is reduced by the same integral multiple M from the number of phases characteristically produced by a timing reference signal generator operating at a characteristic frequency substantially equal to the desired output clock frequency. A MUX is used thereafter to select between and among the multi-phase signals in accordance with a phase control word, the phase control word changing states in accordance with a Gray code sequence.

According to this configuration, the timing reference signal generator is operating at a frequency M times higher than the required output clock frequency. Because of this higher frequency, and the arrangement of elements according to the present invention, the number of output phases that needs to be provided by the generator can be reduced by the same integral multiple M. The generator and MUX serve to define an output signal having a particular desired phase state. Additionally, a divide-by-M frequency divider serves to provide the particular phase date signal at the appropriate output frequency.

The high speed timing signal generator of the present invention is able to develop a significantly larger number of transition edges within an output clock period than a relatively lower speed device. This allows the number of physical output taps to be reduced by the same integral multiple M, while retaining the same phase resolution granularity of the relatively lower speed system.

Rejections under 35 U.S.C. 103(a)

Claims 3, and 8-11

The Examiner rejected Claims 3, 8-11, and 19-22 under 35 USC 103(a) as being unpatentable over Ghoshal (USP 5,068,628) in view of Hsu (USP 5,805,003) and Barrett et al. (USP 5,243,599).

The Examiner states as to Claim 8 that Ghoshal shows in Figure 2 a phase lock loop comprising: a detector (76) for comparing a phase or frequency characteristic of an input signal (26) to a phase or frequency characteristic of a timing reference signal (74); a timing reference signal generator (46, 48, 56, ..., 78), connected in feedback fashion to provide a timing reference signal to the detector. The Examiner then states that Figure 2 shows all of the elements of the Claim except for the timing reference signal generator being operatively configured to produce an output signal at a characteristic frequency an integral multiple of a desired output clock frequency. The Examiner then states that Hsu shows in Figure 1 a frequency divider circuit (/M) for reducing the output frequency. The Examiner states that it would have been obvious to one having ordinary skill in the art to add a frequency divider circuit to the output of Ghoshal's Figure 2 for the purpose of reducing the output frequency. The Examiner then states that this combination shows all the elements of Claim 8 except for the phase select MUX being a Gray code MUX. The Examiner then cites Barrett as showing in Figure 3 a Gray code MUX with the advantage of providing a faster control path than other types of decode devices. The Examiner then states that it would have been obvious to one having ordinary skill in the art to employ the teaching of Barrett into the Ghoshal MUX for the purpose of having a faster control path.

As to Claim 3, the Examiner states that Ghoshal's Figure 2 shows a block which further comprises a loop filter. As to Claim 9, the Examiner states that Barrett's Figure 3 shows the phase control word having a characteristic width J, where J is mathematically dependent on the frequency of the scale factor M. As to Claim 10, the Examiner states that it is an obvious design choice for selecting a frequency divider circuit to be constructed of current mode logic components dependent upon particular environment of use to ensure optimum performance. As to Claim 11, the Examiner states that it is an obvious design choice for selecting a phase control MUX to be constructed of current mode logic components dependent upon a particular environment of use to ensure optimum performance.

The Applicants respectfully traverses these rejections.

A telephone conversation with the Examiner on January 8, 2002, leads the Applicants to believe that further clarification of the invention over the cited prior art is needed in order to obtain allowability of the claims.

Accordingly, Claim 8 has been amended to include the elements of Claim 3, with Claim 3 being deleted. Claim 8 now includes the loop filter coupled between the phase/frequency detector and the timing reference generator, wherein the loop filter serves to develop a control voltage for the timing reference generator. In Claim 8, certain elements pertaining to the operative configuration of the timing reference signal generator are further clarified, namely the timing reference generator is configured to:

(a) produce an output signal at a characteristic frequency an integral multiple M of a desired output clock frequency, whereby the higher output frequency reduces, by the same integral multiple M, the number of output phases to be provided by the timing reference signal generator, and

(b) utilize the loop filter to facilitate the output of multi-phase signals, each phase signal oscillating at the characteristic frequency, whereby the number of phases represented by the multi-phase output signals is reduced by the integral multiple M from a number of phases produced by a timing reference signal

generator operating at a characteristic frequency substantially equal to a desired output clock frequency.

It is believed that the full combination of elements, and the functionality so provided, are unique over the cited prior art. The Examiner cites Hsu as providing an "M divider" and then states that the combination of such a divider with the elements of Ghoshal would render the present invention obvious. It should be noted that Ghoshal does not teach or suggest (either alone or in combination with other cited art) using an output signal that has been increased by an integral multiple M. Ghoshal also does not teach or suggest (either alone or in combination with other cited art) that certain increases in the output signal frequency serve to reduce, by the same integral multiple M, the number of output phases to be provided by the timing reference signal generator. Ghoshal also does not teach or suggest (either alone or in combination with other cited art) that using the loop filter to facilitate the output of multi-phase signals, with each phase signal oscillating at the characteristic frequency, produces a result whereby the number of phases represented by the multi-phase output signals is reduced by the integral multiple M from a number of phases produced by a timing reference signal generator operating at a characteristic frequency substantially equal to a desired output clock frequency.

Hsu is then cited as teaching a divider circuit. Hsu describes the divider circuit in terms of providing a second base frequency. A first frequency is multiplied by a factor N, and then divided by a factor M to get the second desired frequency, which is an N/M multiple of the first frequency. While it might be obvious (from any such reference) to take a frequency and divide it (using a divider) in order to simply produce a lessor frequency, it is maintained by the Applicants that this simple operation does not render the present invention obvious in light of Ghoshal. The present invention does more than simply divide the output frequency, after having multiplied it, as described above.

The present invention further adds elements including a frequency divider circuit, and the phase select MUX. In addition to the arguments cited above, the Applicants

believe these elements further render the invention patentably distinct over the cited prior art, either alone or in combination. The multi-phase output signals are reduced by the same integral multiple M, and the MUX serves to select from among these phases.

Claim 9 further provides for the control word of the phase control word having a characteristic width J, where J is mathematically dependent on the frequency scale factor M. In particular, the unique arrangement of elements above further relates to the same integer multiple M via reduction of the physical size of the phase control selection MUX by the factor M. The number of phase control lines is represented mathematically by a value J = Kx (log2/logM). This relationship, in light of the differences cited above, is believed to be unique over the cited prior art.

Claims 10 and 11 further provide limitations on certain device construction being of current mode logic components. It is believed that these limitations further render the claimed invention patentably distinct over the cited prior art.

Accordingly, the Applicants respectfully request that the rejections to Claims 8-11 be withdrawn, in light of the amendments herein, and the arguments cited above.

<u>Claims 19, 21, and 22</u>

The Examiner next rejected Claims 21 and 22 as reciting similar limitations as Claims 8-11 and rejected the claims for the same reasons cited above. As to Claim 19, the Examiner stated that the references Ghoshal and Hsu teach the number of phases represented by multi-phase output signals as being reduced by a scale factor M from a number of phases produced by a timing reference signal generator operation at a characteristic frequency substantially equal to a desired output clock frequency. As to Claim 20, the Examiner states that Ghoshal's Figure 2 shows a phase select MUX (78), the phase select MUX selecting between and among the multi-phase signals to define a respective one as an output clock signal.

The Applicants respectfully traverse these rejections.

The elements of Claim 19 have been combined into Claim 21, and Claim 19 has been deleted. Claim 21 is believed to be unique for at least the reasons above pertaining to amended Claim 8. Despite the arguments made above by the Examiner, it is believed that Claim 21, as now amended, is unique over the prior art. Ghoshal, in combination with Hsu, is not believed to provide the present invention. Claim 22 further adds the uniqueness of the control word being mathematically related to the same integer multiple M, as discussed in detail above.

Claim 20 was cancelled in a prior amendment.

Accordingly, the Applicants respectfully request that the rejections to Claims 21 and 22 be withdrawn, in light of the amendments herein, and the arguments cited above.

CONCLUSION

The Applicants respectfully request allowance of these claims, in light of the Final rejections cited against the claims. It is believed that the case is in present condition for allowance, and an appeal should not be necessary. The Examiner is encouraged to contact the attorney and/or firm below if this would further the allowance of the case.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

(Unchanged Claims are included for reference purposes)

8. (Twice Amended) A phase lock loop comprising:

a detector for comparing a phase or frequency characteristic of an input signal to a phase or frequency characteristic of a timing reference signal;

a timing reference signal generator, connected in feedback fashion to provide a timing reference signal to the detector[,];

a loop filter coupled between the detector and the timing reference generator, the loop filter developing a control voltage for controlling the operational frequency of the timing reference generator,

wherein the timing reference signal generator [being] is operatively configured to:

(a) produce an output signal at a characteristic frequency an integral multiple M of a desired output clock frequency [and to produce an output signal at a characteristic frequency M times the frequency of a desired output clock frequency], whereby the higher output frequency reduces, by the same integral multiple M, the number of output phases to be provided by the timing reference signal generator, and

[being constructed to] (b) utilize the loop filter to facilitate the output of multi-phase signals, each phase signal oscillating at the characteristic frequency, [wherein] whereby the number of phases represented by the multi-phase output signals are reduced by [a scale factor] the integral multiple M from a number of phases produced by a timing reference signal generator operating at a characteristic frequency substantially equal to a desired output clock frequency;

a frequency divider circuit coupled to receive the output signal and reduce its characteristic frequency to a desired output clock frequency; and

a phase select MUX, the phase select MUX selecting between and among the multi-phase signals to define a respective one as an output clock signal, the phase select MUX being a Gray code MUX, the MUX selecting between and among multi-phase signals in accordance with a phase control word, the phase control word changing states

in accordance with a Gray code sequence for reducing jitter when the phase control word change states.

9. (Unchanged) The phase lock loop according to claim 8, wherein the phase control word has a characteristic width J, where J is mathematically dependent on the frequency scale factor M.

10. (Unchanged) The phase lock loop according to claim 9, wherein the frequency divider circuit is constructed of current mode logic components.

11. (Unchanged) The phase lock loop according to claim 9, wherein the phase control MUX is constructed of current mode logic components.

21. (Twice Amended) A feedback controlled timing circuit, comprising:

a comparison circuit configured to compare a frequency characteristic of an input signal to a frequency characteristic of a timing reference signal, the comparison circuit asserting control signals in response to said comparison;

a timing reference signal generator, connected to provide a timing reference signal to the comparison circuit, the timing reference signal generator responsive, in feedback fashion, to said control signals asserted by the comparison circuit, the timing reference signal generator being configured to develop an output signal at a frequency an integral factor M times the frequency of a desired output clock signal, the desired output clock signal having a frequency characteristic an integral factor N times the frequency characteristic of the input signal, the timing reference signal generator being implemented as a VCO, the VCO constructed as a sequential delay stage and developing multi-phase output signals, each oscillating at the characteristic frequency of the VCO, and each having a phase relationship characterized by an inherent delay of each delay stage whereby the number of phases represented by the multi-phase output signals are reduced by the integral factor M from a number of phases produced by a timing reference signal generator operating at a characteristic frequency substantially equal to a desired output clock frequency;

first frequency divider circuitry disposed between the timing reference signal generator and the comparison circuit, the first frequency divider circuitry dividing the

output signal of the timing reference signal generator by a scale factor (NxM) to develop said frequency characteristic provided to said comparison circuit;

second frequency divider circuitry disposed between the timing reference signal generator and an output, wherein the first and second frequency divider circuitry having different frequency division characteristics, the second frequency divider circuitry dividing the output signal of the timing reference signal generator by a scale factor M to develop said desired output clock signal; and

a phase select MUX, the phase select MUX selecting between and among the multi-phase signals to define a respective one as an output clock signal, the phase select MUX being a Gray code MUX, the MUX selecting between and among multi-phase signals in accordance with a phase control word, the phase control word changing states in accordance with a Gray code sequence for reducing jitter when the phase control word change states.

22. (Unchanged) The timing circuit according to claim 21, wherein the phase control word has a characteristic width J, where J is mathematically dependent on the frequency scale factor M.